IN THE CLAIMS:

Please enter the following claim set:

1. (currently amended) A method for manufacturing a semiconductor device, the method comprising the steps of:

(a) forming a gate dielectric layer on a semiconductor layer;

(b) forming a first conductive layer having a specified pattern on the gate dielectric layer;

(c) forming sidewall insulation layers on side walls of the first conductive layer;

(d) forming a source region and a drain region in the semiconductor layer;

(e) depositing a first insulation layer that covers the first conductive layer and the sidewall insulation layers, the first insulation layer comprising a material different from that of the sidewall insulation layers;

(f) planarizing the first insulation layer until an upper surface of the first conductive layer is exposed;

(g) removing a part of the first conductive layer between the sidewall insulation layers in a manner that the gate dielectric layer is not exposed to thereby form a recessed section on the first conductive layer between the sidewall insulation layers;

(h) partially filling the recessed section between the sidewall insulation layers with a second conductive layer to form a gate electrode that includes at least the first conductive layer and the second conductive layer;

(i) forming a second insulation layer that fills the recessed section between the sidewall insulation layers on the second conductive layer, the second insulation layer comprising a material different from that of the first insulation layer;

(j) etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

(k) forming a first contact layer in the first through hole.

2. (previously presented) A method for manufacturing a semiconductor device according to claim 1, wherein, in the step (j), the second insulation layer and the sidewall insulation layers comprise a material that is more resistant to an etchant than the first insulation layer.

3. (previously presented) A method for manufacturing a semiconductor device according to claim 1, wherein the first conductive layer is a silicon layer, and the step (h) includes the steps of

(h – 1) depositing a metal layer for siliciding the first conductive layer on the first conductive layer; and

(h – 2) siliciding the first conductive layer to form a silicide layer.

4. (previously presented) A method for manufacturing a semiconductor device according to claim 1, further comprising:

(l) forming a third insulation layer on the first insulation layer and the second insulation layer;

(m) etching the third insulation layer to form a second through hole; and

(n) forming a second contact layer in the second through hole, wherein the second through hole overlaps the first through hole.

5. (canceled)

6. (original) A method for manufacturing a semiconductor device according to claim 1, wherein the first insulation layer comprises silicon oxide and the second insulation layer comprises silicon nitride.

7. (canceled)

8. (original) A method for manufacturing a semiconductor device according to claim 1, wherein the first insulation layer comprises silicon oxide and the sidewall insulation layers comprise silicon nitride.

9. (currently amended) A method for manufacturing a semiconductor device, comprising:

forming a gate dielectric layer on a semiconductor layer;

forming a first conductive layer having a specified pattern on the gate dielectric layer;

forming sidewall insulation layers on side walls of the first conductive layer;

forming a source region and a drain region in the semiconductor layer;

removing a part of the first conductive layer between the sidewall insulation layers in a manner so that the gate dielectric layer is not exposed and a portion of the first conductive layer remains on the gate dielectric layer between the sidewall insulation layers, to thereby form a recessed section ~~on the first conductive layer~~ between the sidewall insulation layers, wherein the removing a part of the first conductive layer is carried out after formation of the source region and the drain region;

forming a second conductive layer in a portion of the recessed section on the portion of the first conductive layer that remains between the sidewall insulation layers; and

forming an insulation layer in the recessed section on the second conductive layer between the sidewall insulation layers.

10. (previously presented) A method for manufacturing a semiconductor device according to claim 9, further comprising, after forming the source region and the drain region and before removing a part of the first conductive layer:

forming a first insulating layer that covers the first conductive layer, the sidewall insulation layers, and the semiconductor layer; and

planarizing the first insulation layer so that the first conductive layer is exposed.

11. (previously presented) A method for manufacturing a semiconductor device according to claim 10, further comprising, after forming the insulation layer in the recessed section above the second conductive layer:

etching the first insulation layer to form a first through hole that reaches the source region or the drain region; and

forming a first contact layer in the first through hole.

12. (previously presented) A method for manufacturing a semiconductor device according to claim 9, wherein the second conductive layer comprises a silicide.

13. (previously presented) A method for manufacturing a semiconductor device according to claim 9, wherein the removing a part of the first conductive layer further includes removing a greater depth of the first conductive layer from a center region than from end regions adjacent to the sidewall insulation layers.

14-23. (canceled)

24. (previously presented) A method for manufacturing a semiconductor device according to claim 9, wherein the first insulation layer comprises silicon oxide, and the second insulation layer comprises silicon nitride.

25. (new) A method for manufacturing a semiconductor device, comprising:

forming a gate dielectric layer on a semiconductor layer;

forming a first conductive layer having a specified pattern on the gate dielectric layer;

after the forming the first conductive layer having a specified pattern on the gate dielectric layer, forming sidewall insulation layers on side walls of the first conductive layer so that the first conductive layer in its entirety is positioned between the sidewall insulation layers;

after forming the sidewall insulation layers, removing a first portion of the first conductive layer between the sidewall insulation layers in a manner so that a second portion of the first conductive layer remains between on the gate dielectric layer between the sidewall

insulation layers and a gap remains above the second portion of the first conductive layer between the sidewall insulation layers;

forming a second conductive layer on the second portion of the first conductive layer and removing a first portion of the second conductive layer so that a second portion of the second conductive layer remains on the first conductive layer between the sidewall insulation layers, wherein the second portion of the second conductive layer does not entirely fill the gap between the sidewall insulation layers; and

forming an insulation layer on the second portion of the second conductive layer to fill the gap between the sidewall insulation layers.

26. (new) A method for manufacturing a semiconductor device according to claim 25, wherein the first conductive layer comprises polycrystalline silicon and the second conductive layer comprises a material selected from the group consisting of a metal and a compound of metal and silicon.

27. (new) A method for manufacturing a semiconductor device according to claim 25, wherein the second conductive layer includes at least one metal selected from the group consisting of W, Al, and Cu.

28. (new) A method for manufacturing a semiconductor device according to claim 25, wherein the second conductive layer comprises a silicide.

29. (new) A method for manufacturing a semiconductor device according to claim 25, further comprising forming the sidewall insulation layers from silicon nitride and in direct contact with the first conductive layer.

30. (new) A method for manufacturing a semiconductor device according to claim 25, wherein the removing a first portion of the first conductive layer between the sidewall insulation layers further includes removing a greater depth of the first conductive layer from a center region than from end regions adjacent to the sidewall insulation layers.